WHAT IS CLAIMED IS:

1. A method for producing a circuit board having an integrated electronic component comprising:

providing a circuit board substrate having a first substrate surface and a second substrate surface;

securing a first integrated electronic component to the first substrate surface;

disposing a first dielectric layer on the first substrate surface and over the first integrated electronic component;

disposing a metallic layer on the first dielectric layer to produce an integrated electronic component assembly;

producing in the integrated electronic component assembly at least one via having a metal lining in contact with said metallic layer;

disposing a second dielectric layer over said via and over said metallic layer;

producing at least one opening in the second dielectric layer and in the first dielectric layer to expose at least part of the first integrated electronic component; and

forming a metal lining in said opening and coupled to the first integrated electronic component to produce a circuit board having at least one integrated electronic component.

2. The method of Claim 1 wherein said circuit board substrate includes a first metallic layer disposed on said first substrate surface and a second metallic layer disposed on said second substrate surface;

3. The method of Claim 1 wherein said circuit board substrate comprises a multi-layer core substrate.

4. The method of Claim 2 wherein said circuit board substrate comprises a multi-layer core substrate.

5. The method of Claim 1 wherein said circuit board substrate includes said at least one via passing through said circuit board from said first substrate surface to said second substrate surface.

6. The method of Claim 2 wherein said circuit board substrate includes said at least one via passing through said circuit board from said first substrate surface to said second substrate surface.

7. The method of Claim 3 wherein said circuit board substrate includes said at least one via passing through said circuit board from said first substrate surface to said second substrate surface.

8. The method of Claim 2 additionally comprising patterning said first metallic layer to expose at least a portion of said first substrate surface, said first integrated electronic component being secured to said portion of said first substrate surface.

9. The method of Claim 8 additionally comprising patterning said second metallic layer to expose at least a portion of said second substrate surface.

10. The method of Claim 9 additionally comprising connecting a second integrated electronic component to said portion of said second substrate surface.

11. The method of Claim 9 additionally comprising forming a cavity in said portion of said second substrate surface, and disposing a second integrated electronic component in said cavity.

12. The method of Claim 1 wherein said first integrated electronic component includes at least one first pad in contact with said metal lining in said opening.

13. The method of Claim 1 additionally comprising producing in the integrated electronic component assembly at least one blind via through said metallic layer and through said first dielectric layer, said blind via being lined with a metal via which is coupled to said metallic layer.

14. The method of Claim 1 wherein said via extends entirely through the integrated electronic component assembly.

15. The method of Claim 13 wherein said via extends entirely through the integrated electronic component assembly.

16. The method of Claim 8 additionally comprising disposing a patterned metallic layer over the second dielectric layer.

17. A multi-layer printed circuit board having at least one prefabricated integrated electronic component comprising a circuit board substrate having a first substrate surface and a second substrate surface; a first integrated electronic component secured to the first substrate surface; a first dielectric layer disposed on the first substrate surface and over the first integrated electronic component; a metallic layer disposed on the first dielectric layer; at least one via passing through the first dielectric layer and having a metal lining in contact with said metallic layer; and a second dielectric layer disposed over said via and over said metallic layer, said first dielectric layer and said second dielectric layer having a structure defining at least one opening exposing at least part of the first integrated electronic component, said opening supporting an opening metal lining which is coupled to the first integrated electronic component.

18. The multi-layer printed circuit board of Claim 17 additionally comprising a first metallic layer disposed on the said first substrate surface and a second metallic layer disposed on said second substrate surface.

19. The multilayer printed circuit board of Claim 17 wherein said circuit board substrate comprises a multi-layer core substrate.

20. The multilayer printed circuit board of Claim 17 wherein said at least one via passes from said first substrate surface to said second substrate surface.

21. The multilayer printed circuit board of Claim 18 wherein said at least one via passes from said first substrate surface to said second substrate surface.

22. The multilayer printed circuit board of Claim 18 wherein said first metallic layer comprises a patterned first metallic layer to expose at least a portion of said first substrate surface, said first integrated electronic component being secured to said exposed portion of said first substrate surface.

23. The multilayer printed circuit board of Claim 18 wherein said second metallic layer comprises a patterned second metallic layer to expose at least a portion of said second substrate surface.

24. The multilayer printed circuit board of Claim 23 additionally comprising a second integrated electronic component secured to said exposed portion of said second substrate surface.

25. The multilayer printed circuit board of Claim 23 wherein said exposed portion of said second substrate surface includes a cavity.

26. The multilayer printed circuit board of Claim 25 additionally comprising a second integrated electronic component disposed in said cavity.

27. The multilayer printed circuit board of Claim 17 additionally comprising at least one first pad disposed on said first integrated electronic component and contacting said metallic layer.

28. The multilayer printed circuit board of Claim 25 additionally comprising at least one first pad disposed on said first integrated electronic component and contacting said metallic layer.

29. The multilayer printed circuit board of Claim 26 additionally comprising at least one first pad disposed on said first integrated electronic component and contacting said metallic layer.

30. The multilayer printed circuit board of Claim 17 additionally comprising at least one metal-lined via extending through said metallic layer and through said first dielectric layer.

31. The multilayer printed circuit board of Claim 25 additionally comprising at least one metal-lined via extending through said metallic layer and through said first dielectric layer.

32. The multilayer printed circuit board of Claim 26 additionally comprising at least one metal-lined via extending through said metallic layer and through said first dielectric layer.

33. The multilayer printed circuit board of Claim 27 additionally comprising at least one metal-lined via extending through said metallic layer and through said first dielectric layer.

34. The multilayer printed circuit board of Claim 33 additionally comprising a patterned metal layer disposed on said second dielectric layer.

35. A method for producing a circuit board having an integrated electronic component comprising:

providing a circuit board substrate having a first substrate surface and a second substrate surface;

securing a first integrated electronic component to the first substrate surface;

disposing a first dielectric layer on the first substrate surface and over the first integrated electronic component;

producing at least one via;

disposing a metallic layer on the first dielectric layer and in the via to produce an integrated electronic component assembly;

disposing a second dielectric layer over said metallic layer;

producing at least one opening in the second dielectric layer and in the first dielectric layer to expose at least part of the first integrated electronic component; and

forming a metal lining in said opening and coupled to the first integrated electronic component to produce a circuit board having at least one integrated electronic component.